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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,110	10/26/2001	Tod David Wolf	TI-33162	7695

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EXAMINER	
ABRAHAM, ESAW T	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,110	WOLF ET AL.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 24-29* is/are pending in the application.

4a) Of the above claim(s) *11-17* is/are withdrawn from consideration.

5)☒ Claim(s) *18-23* is/are allowed.

6)☒ Claim(s) *1-10 and 24-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to the applicant's amendments

112, 1st paragraph rejection

In view of the amendment filed on 09/02/05, the Examiner withdraws the 112, 1st paragraph rejection to claims 1 and 24.

RCE

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/02/05 has been entered.

1. Claims 1-10, 24-29 remained pending and claims 18-23 are allowed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims **1-10 and 24-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Maru (U.S. PN: 6,516,444).

As per claims **1 and 2,** Maru in figure 2A teach or disclose an output from sum from an adder and a parity sequence are input to two's complement circuits (203 and 204) with control terminals wherein each of the complement circuits (203 and 204) has a function of calculating two's complement of input data or directly outputting the value of input data in accordance with the signal level of the control terminal and a most significant bit (201) representing the polarity of input data is input to the control terminals of the complement circuits (203 and 204) (see col. 4, lines 40-64). Further, Maru teaches that with this function, outputs from the complement circuits output negative values while holding their absolute values (see col. 4, lines 40-64). Maru **does not explicitly teach** a method of adjusting values when the values are within predetermined proximity. **However,** Maru teaches a method of combining output values from complement circuits (203 and 204) coupled by an adder (205) and further selected by four selectors (206-209) to enable selection and combinations are selected by a most significant bit (202) representing the polarity of input data (see col. 5, lines 32-45). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made

to adjust the output values of the two's complement by using an adder and selectors. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because adjusting values, which are within proximity, would guarantee accurate operations. Maru **does not explicitly** disclose the method of adjusting operand values in order to avoid crossover from maximum positive value to maximum negative value. Nevertheless, as would have been well known to one ordinary skill in the art at the time the invention was made, such methods of adjustment are required to control the operands operation. Accordingly, it would have been obvious to one ordinary skill in the art to adjust operand values because such methods of adjustment would have been required in order improve and heighten the decoding efficiency.

As per claims **3 and 4,** Maru teach all the subject matter claimed in claim 1 including the complement circuits (203 and 204) has a function of calculating two's complement of input data or directly outputting the value of input data in accordance with the signal level of the control terminal and a most significant bit (201) representing the polarity of input data is input to the control terminals of the complement circuits (203 and 204) (see col. 4, lines 40-64).

As per claims **5 and 6,** Maru teach all the subject matter claimed in claim 1 including in figure 2A teach an adder (205) for adding values.

As per claims **7 and 8,** Maru teach all the subject matter claimed in claim 1 including in figure 8 teach a subtraction circuit for subtracting values (803).

As per claim **9,** Maru teach all the subject matter claimed in claim 1 including in figure 9 a turbo decoder

As per claim **10,** Maru teach all the subject matter claimed in claims 1 and 9 including in figure 9 a turbo decoder comprising an extrinsic information (see an output line from an element 907-1).

As per claims **24-29,** Maru a turbo decoder includes a first reception signal memory for storing an information sequence, a second reception signal memory for storing first and second parity sequences, an a priori memory for storing extrinsic/previous information in repetitive processing and a first adder for adding the information sequence read out first memory and the previous information read out from the a priori memory (see col. 1, lines 41-60) Maru, in figure 2A teach or disclose an output from sum from an adder and a parity sequence are input to two's complement circuits (203 and 204) with control terminals wherein each of the complement circuits (203 and 204) has a function of calculating two's complement of input data or directly outputting the value of input data in accordance with the signal level of the control terminal and a most significant bit (201) representing the polarity of input data is input to the control terminals of the complement circuits (203 and 204) (see col. 4, lines 40-64). Further, Maru teaches that with this function, outputs from the complement circuits output negative values while holding their absolute values (see col. 4, lines 40-64). Maru **does not explicitly teach** a quadrant shifters coupled to an adder. **However,** Maru teaches a method of combining output values from complement circuits (quadrant shifters) coupled by an adder (205) and further selected by four selectors (206-209) to enable selection and combinations are selected by a most significant bit (202) representing the polarity of input data (see col. 5, lines 32-45). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to adjust or identify the output values of the two's complement by using an

adder and selectors. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because adjusting values, which are within proximity, would guarantee accurate operations. Maru **does not explicitly** disclose the method of adjusting operand values in order to avoid crossover from maximum positive value to maximum negative value. Nevertheless, as would have been well known to one ordinary skill in the art at the time the invention was made, such methods of adjustment are required to control the operands operation. Accordingly, it would have been obvious to one ordinary skill in the art to adjust operand values because such methods of adjustment would have been required in order improve and heighten the decoding efficiency.

Examiner's statement for reason for allowance

3. Claims **18-23** have been allowed.

The following is an examiner's statement for allowance:

As per claim18:

The prior art, Maru (U.S. PN: 6,516,444) of record in figure 2A teach or disclose an output from sum form an adder and a parity sequence are input to two's complement circuits (203 and 204) with control terminals wherein each of the complement circuits (203 and 204) has a function of calculating two's complement of input data or directly outputting the value of input data in accordance with the signal level of the control terminal and a most significant bit (201) representing the polarity of input data is input to the control terminals of the complement circuits (203 and 204) (see col. 4, lines 40-64). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious *a* maximum a posteriori decoder, comprising: an

alpha block for producing alpha state metrics in two's complement format; a beta block for producing beta state metrics in two's complement format; an extrinsic block having an input coupled to said alpha block and said beta block for receiving said alpha state metrics and said beta state metrics as operands, said extrinsic block responsive to said operands for producing extrinsic data; and, said extrinsic block including logic coupled to said input for determining, for each operand, whether an original value thrvmnf is within a predetermined proximity of a maximum positive/maximum negative value boundary associated with the two's complement format, and an adjuster coupled to said logic and responsive to a determination by said logic that any of the original operand values is within the predetermined proximity for adjusting all of the original operand values such that cross over from the maximum positive value to the maximum negative value is avoided and to produce respectively corresponding adjusted operand values for use in producing the extrinsic data. Consequently, claim 18 is allowed over the prior art.

Claims **19-23,** which are directly or indirectly dependents of claim 18 are also allowable over the prior art.

Conclusion

3. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Esaw Abraham

Art unit: 2133

GUY LAMARRE
PRIMARY EXAMINER